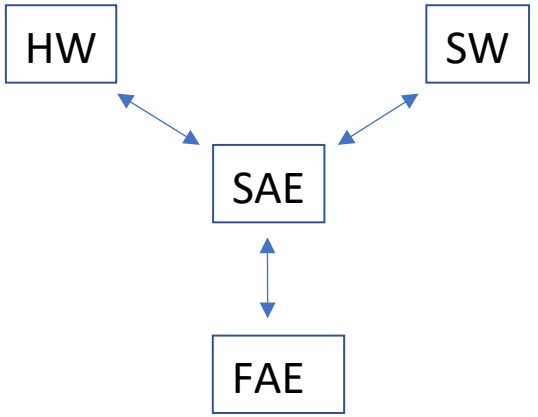
System Application Engineer

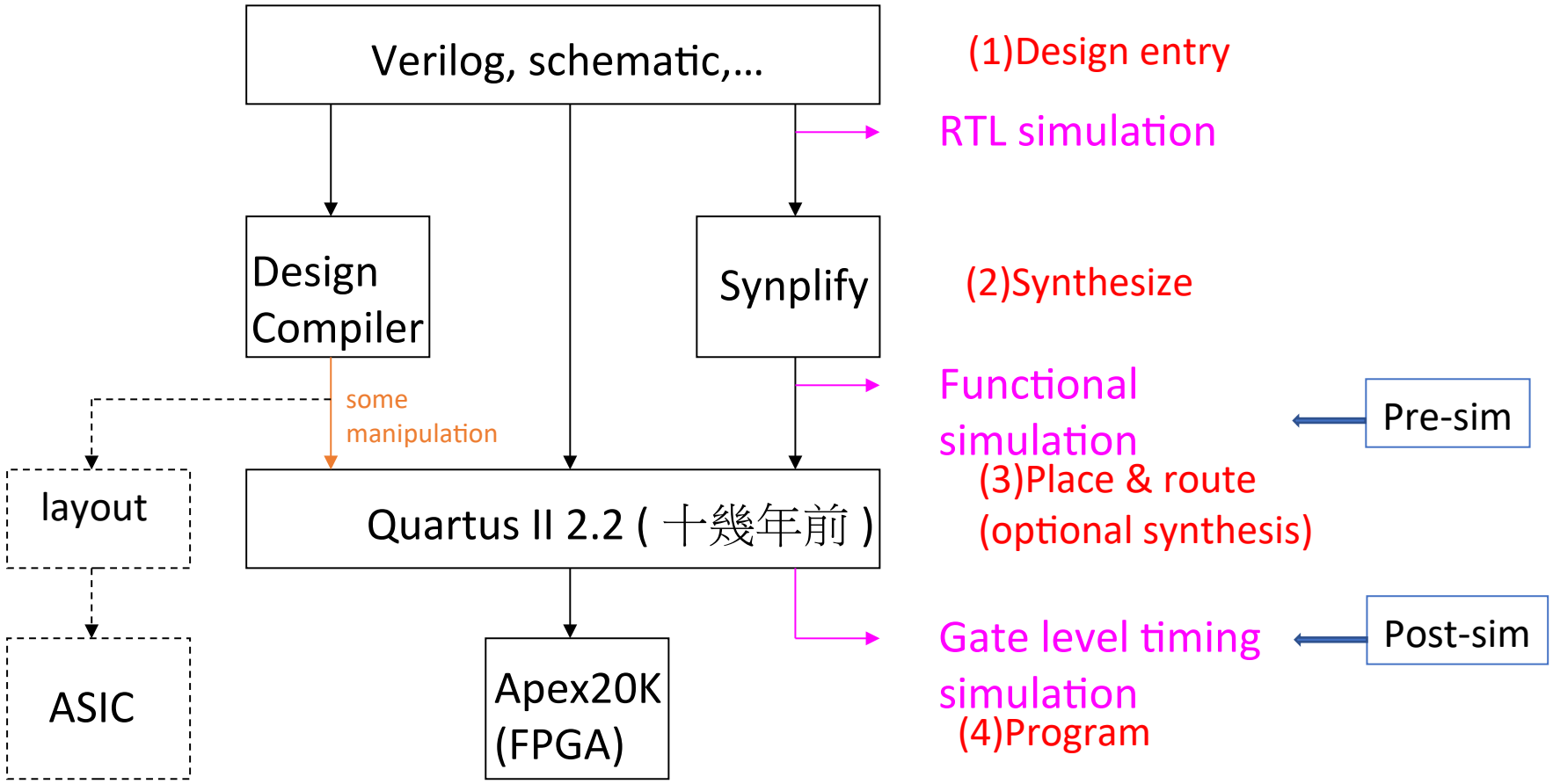
IC 設計的「黑手」？

Research and Development (R&D)

- HardWare (HW, 硬體)
  - **Designer**
    - Digital (數位 , 数字)
    - Analog (類比 , 模拟)
- FirmWare (FW, 韌體)
  - Application Engineer (AE, 應用工程師)
    - System
      - Algorithm(演算法)
      - IC specification, prototype, verification (IC 規格、原型板、驗證)
    - Field (marketing)
- SoftWare (SW, 軟體)



The Design Flow (HW)

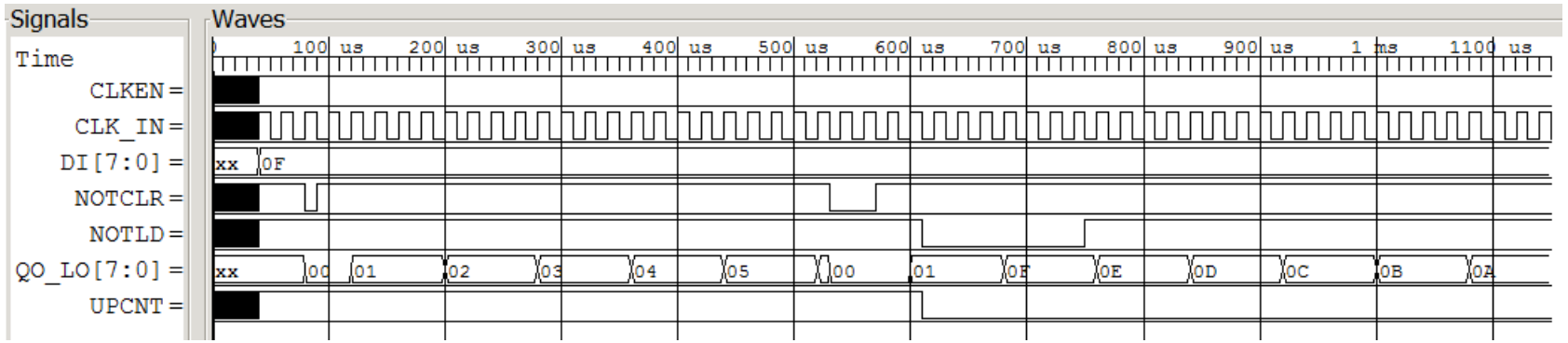


Verilog Source File (HW)

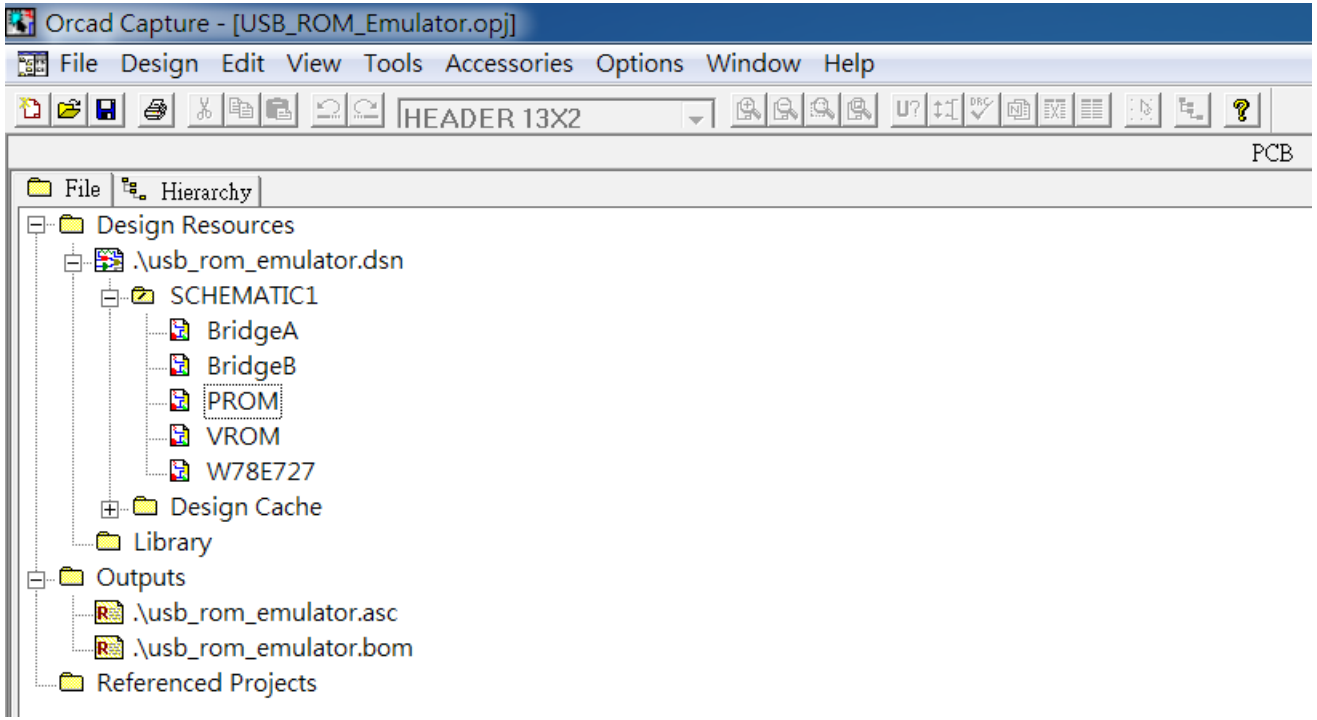
counter.v

```
module counter(NCLR, C, CE, NL, UP, D, Q);

input        NCLR, C, CE, NL, UP;
input  [7:0]  D;
output [7:0]  Q;
reg    [7:0]  QOUT;
reg [21:0] clk_cnt;

//wire clk_gen ;
reg clk_gen ;

always @(negedge NCLR or posedge C)
   begin
      if (NCLR == 1'b0)
         clk_cnt = 22'b00_0000_0000_0000_0000_0000;
      else
        begin
         clk_cnt = clk_cnt + 1 ;
         clk_gen = clk_cnt[1] ;
        end
   end

always @(negedge NCLR or posedge clk_gen)
   begin
      if (NCLR == 1'b0)

            QOUT = 8'b0;
         else if (NL == 1'b0)
            QOUT = D;

            else if (CE == 1'b1)
                  if (UP == 1'b1)
                     QOUT = QOUT + 1'b1;
               else
                     QOUT = QOUT - 1'b1;
   end

assign Q = QOUT;
endmodule
```

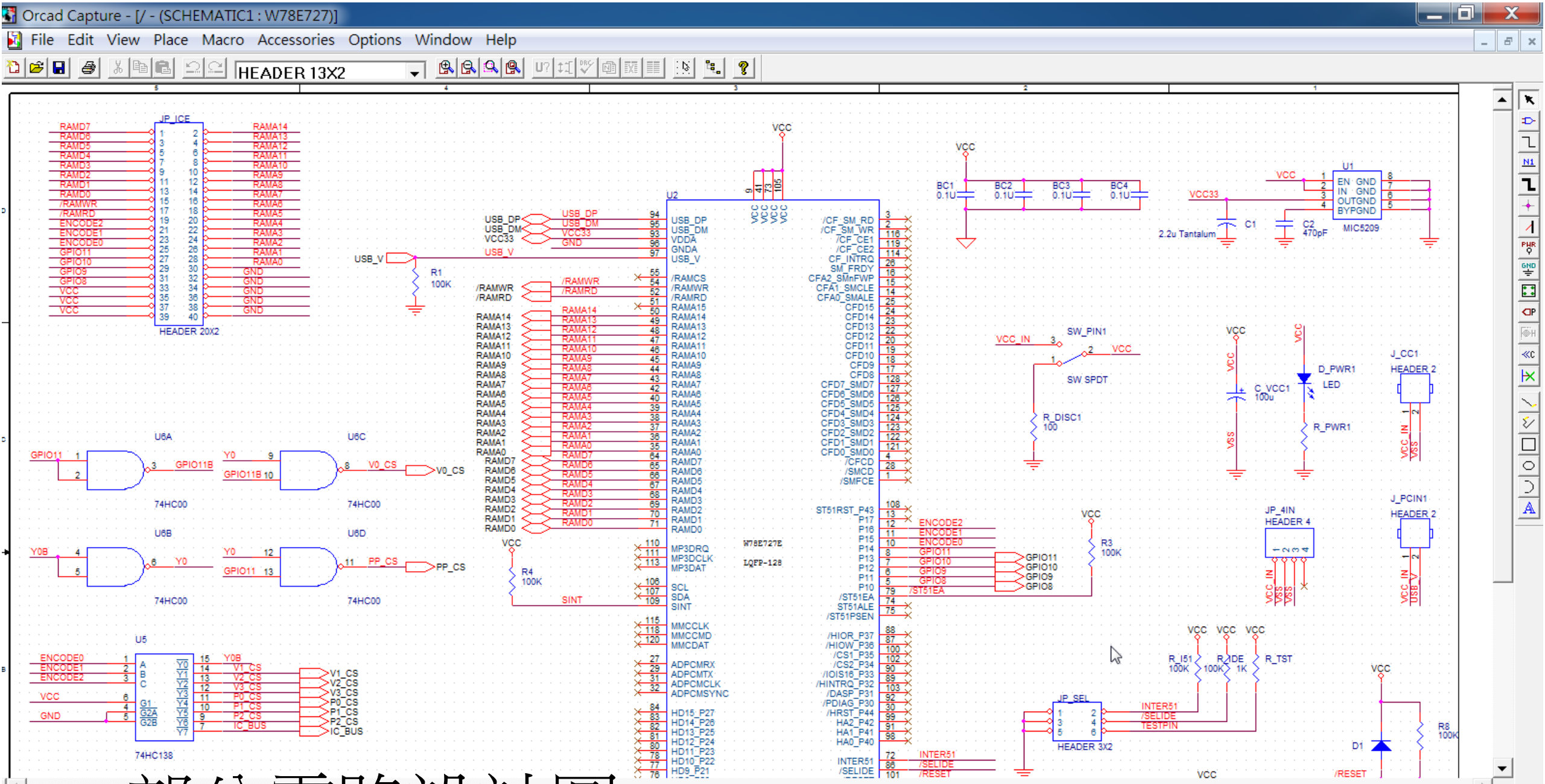
Verilog Simulation (HW)



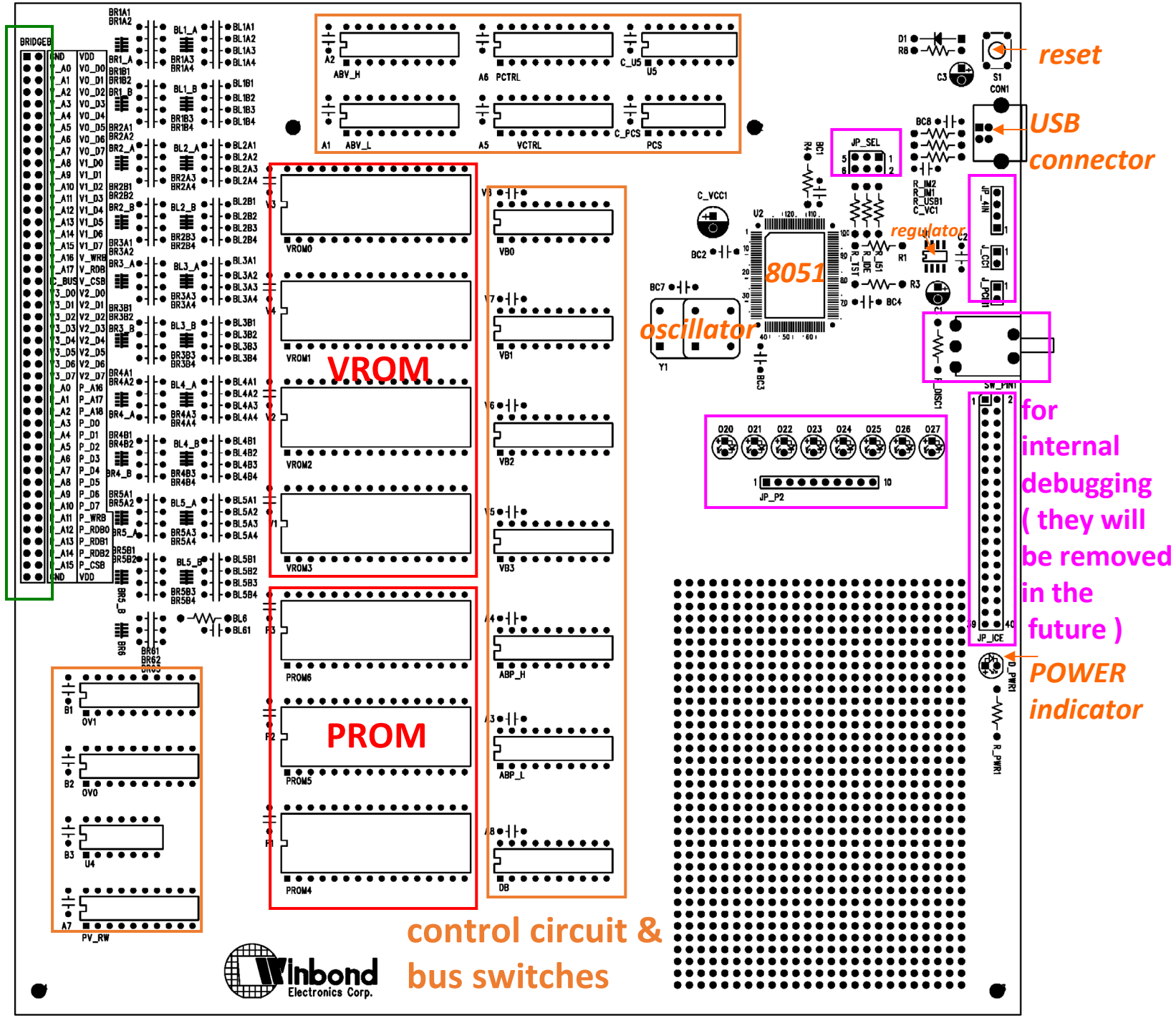
Orcad Design (FW)



給板子 layout 公司的 Orcad project

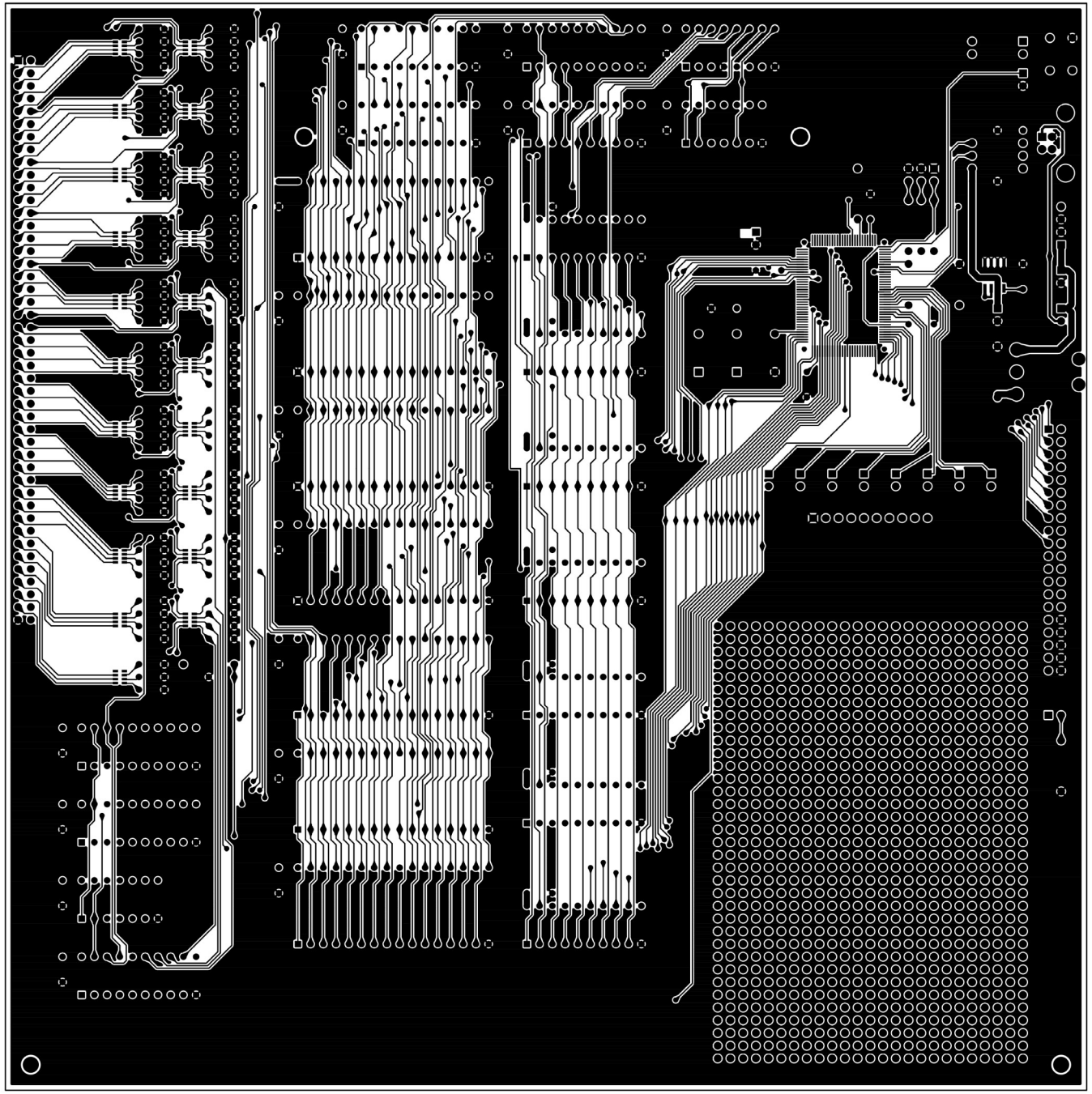

Orcad Capture - [/ - (SCHEMATIC1 : W78E727)]
File Edit View Place Macro Accessories Options Window Help
HEADER 13X2
JP_ICE
HEADER 20X2
U2
W78E727E
LQFP-128
U1
MIC5209
SW_PIN1
SW SPDT
R_DISC1
C_VCC1
D_PWR1
LED
R_PWR1
J_CC1
HEADER 2
J_PCIN1
JP_4IN
HEADER 4
JP_SEL
HEADER 3X2
U6A
U6B
U6C
U6D
74HC00
U5
74HC138
R1
R3
R4
R8
D1
R_I51
R_IDE
R_TST
VCC
VCC33
GND
USB_V
SINT
/RESET
V0_CS
PP_CS
V1_CS
V2_CS
V3_CS
P0_CS
P1_CS
P2_CS
IC_BUS
INTER51
/SELIDE
TESTPIN

部分電路設計圖

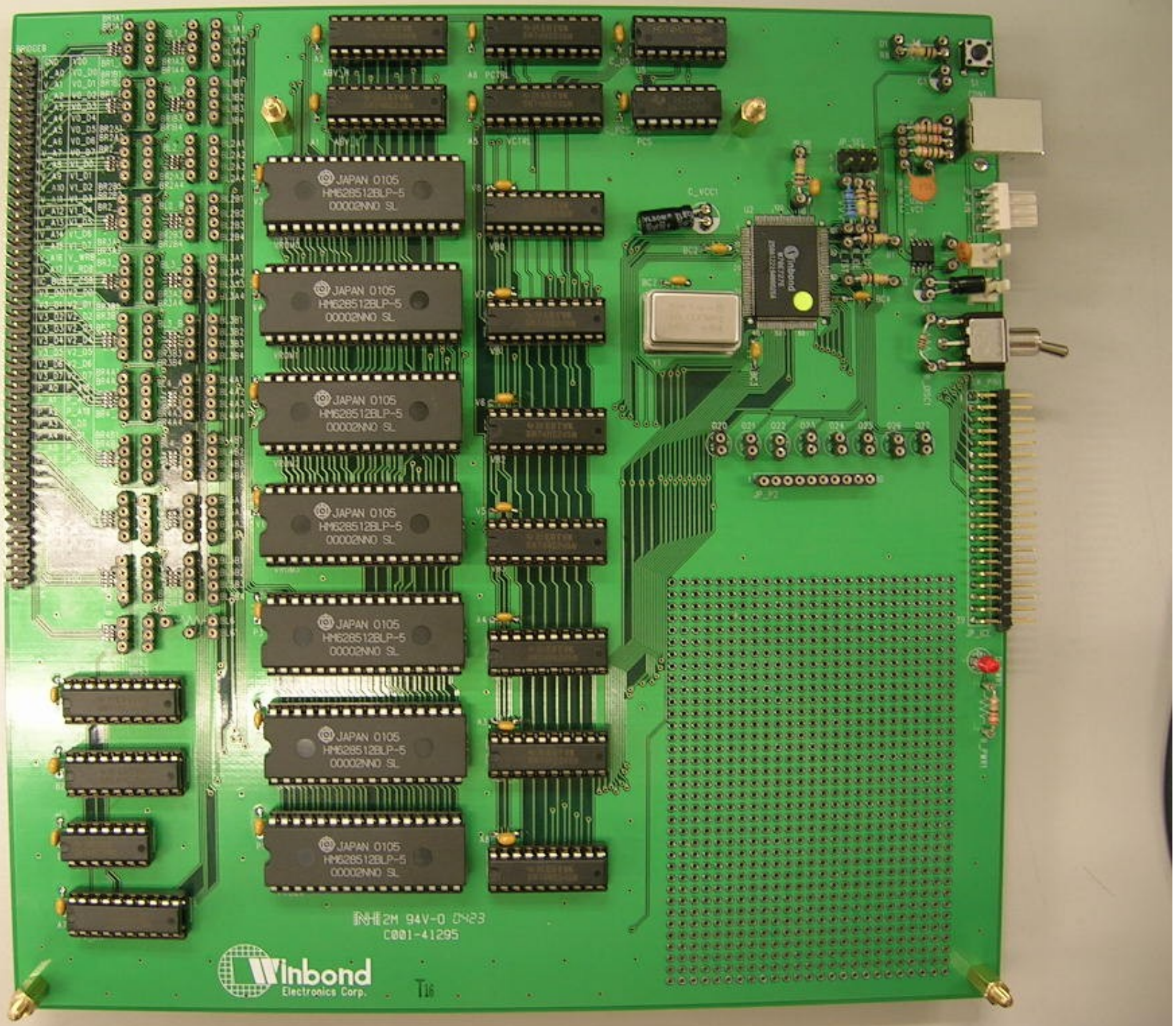

interface
VROM
PROM
8051
oscillator
regulator
reset
USB
connector
for
internal
debugging
(they will
be removed
in the
future)
POWER
indicator
control circuit &
bus switches
Winbond
Electronics Corp.

板子的佈局

板子的走線圖 1/4

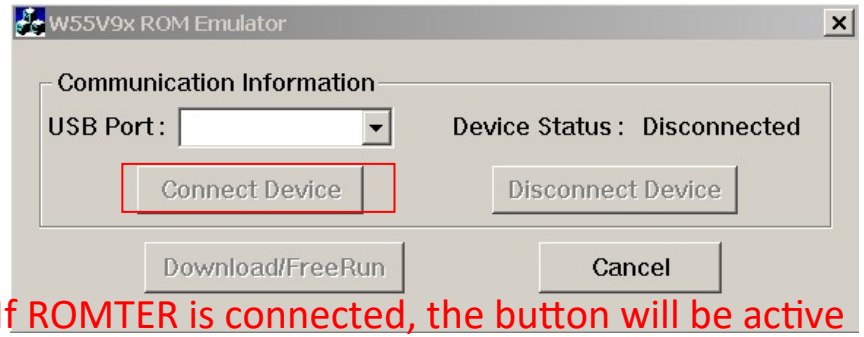


高夫	JOB NAME	USB_ROM	
	LAYER	ARTWORK-TOP	
886-3-5784628	DATE	93-05-18	4 LAYER


JAPAN 0105
HM628512BLP-5
00002NNO SL
Winbond
Electronics Corp.

上好零件的板子

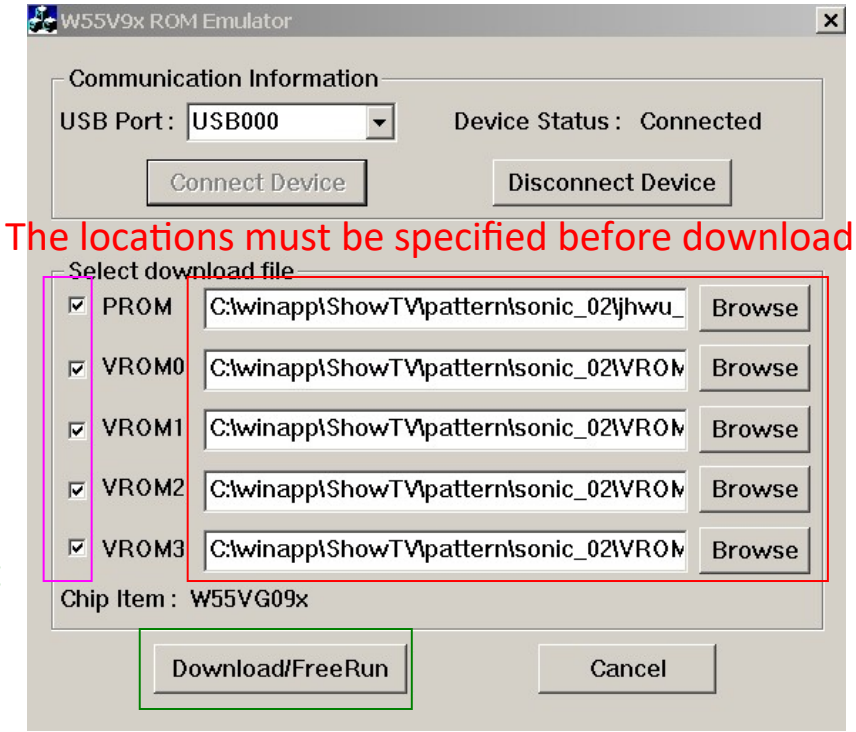
ROM Emulator Tool (SW)



If ROMTER is connected, the button will be active

Download time will be greatly reduced if the ROM file is individually controlled

Don’t forget to press Download-button to start downloading PROM or VROM files



The locations must be specified before downloading

→ This message indicates that all the selected files are already transferred to ROMTER